

In the claims:

1. (currently amended) A method for processing a plurality of independent ~~instructionmulti-~~  
~~packet thread~~ threads comprising: retrieving a first ~~instructionmulti-packet thread-packet~~ from a  
first ~~multi-packet thread-of instructionmulti-packet threads~~; retrieving a second ~~instructionmulti-~~  
~~packet thread-packet~~ from a second ~~multi-packet thread-of instructionmulti-packet threads~~;  
~~executing the first instructionmulti-packet thread~~processing the first packet in a first stage of a  
processing pipeline; and forwarding the first ~~instructionmulti-packet thread packet~~ -to a next  
stage of the processing while forwarding the second ~~instructionmulti-packet thread packet~~ to the  
first stage of the processing pipeline such that the first ~~instructionmulti-packet thread~~ and the  
second ~~instructionmulti-packet thread-packets~~ can be ~~executed~~ processed simultaneously in the  
processing pipeline, and wherein the independence of the ~~instructionmulti-packet threadsmulti-~~  
~~packet~~ -threads eliminates ~~pipeline packet~~ processing delays.

2. (currently amended) The method for processing the plurality of independent ~~instructionmulti-~~  
~~packet thread-multi-packet~~ threads according to claim 1, further comprising: transferring ~~packet~~  
~~data~~ from an input buffer to a packet task manager; dispatching the ~~packet data~~ from the packet  
task manager to an analysis machine; classifying the ~~packet data~~ in the analysis machine; and  
modifying and forwarding the ~~packet data~~ in a packet manipulator.

3. (currently amended) The method for processing the plurality of independent ~~multi-~~  
~~packetinstructionmulti-packet thread~~ threads according to claim 1, further comprising  
transferring the ~~data-packet~~ after modifying and forwarding to an output buffer.

4. (Cancelled)

5. (currently amended) An apparatus for processing a plurality of independent ~~multi-~~  
~~packetinstructionmulti-packet thread~~ threads, said apparatus comprising: a processing pipeline  
including a plurality of stages coupled to receive and process the plurality of independent ~~multi-~~  
~~packetinstructionmulti-packet thread~~ threads such that, during a processing period, each of the  
plurality of stages of the processing pipeline is operating on a different one of the ~~multi-~~

6 ~~packet~~~~instruction~~multi-packet thread threads from the plurality of ~~instruction~~~~multi-packet thread~~  
7 threads, and wherein the independence of the ~~instruction~~~~multi-packet threads~~ threads eliminates  
8 pipeline processing delays.

1 6. (original) The apparatus according to claim 5, further comprising: an analysis machine having  
2 multiple pipelines, wherein one pipeline is dedicated to directly manipulating individual data bits  
3 of a bit field; a packet task manager operationally connected to said analysis machine; and, a  
4 packet manipulator operationally connected to said analysis machine.

1 7. (original) The apparatus according to claim 6, wherein said analysis machine is multi-threaded.

1 8. (original) The apparatus according to claim 6, wherein said analysis machine has 32 threads.

1 9. (original) The apparatus according to claim 6, further comprising: a packet task manager  
2 operationally connected to said analysis machine; a packet manipulator operationally connected  
3 to said analysis machine; and a global access bus including a master request bus and a slave  
4 request bus separated from each other and pipelined.

1 10. (original) The apparatus according to claim 6, further comprising: an external memory engine  
2 operationally connected to said analysis machine; and a hash engine operationally connected to  
3 said analysis machine.

1 11. (previously presented) The apparatus according to claim 9, further comprising: packet input  
2 global access bus program code , stored in a computer readable memory and operable when  
3 executed to control a flow of data packet information from a flexible input data buffer to the  
4 analysis machine.

1 12. (previously presented) The apparatus according to claim 9, further comprising: packet data  
2 global access bus program code, stored in a computer readable memory and operable when

3     executed to control a flow of packet data between a flexible data input bus and the packet  
4     manipulator.

1     13. (previously presented) The apparatus according to claim 9, further comprising: statistics data  
2     global access bus software code used for connection of the analysis machine to the packet  
3     manipulator.

1     14. (previously presented) The apparatus according to claim 9, further comprising: private data  
2     global access bus software code used for connection of the analysis machine to an internal  
3     memory engine submodule.

1     15. (previously presented) The apparatus according to claim 9, further comprising: lookup global  
2     access bus software code used for connection of the analysis machine to an internal memory  
3     engine submodule.

1     16. (original) The apparatus according to claim 9, further comprising: results global access bus  
2     software code used for providing flexible access to an external memory.

1     17. (currently amended) The apparatus according to claim 5, wherein associated with each  
2     ~~instruction~~multi-packet thread is a thread identifier (TID) identifying a subset registers allocated  
3     to the corresponding independent ~~instruction~~multi-packet thread, the subset of registers selected  
4     from among a set of registers, and wherein the subsets associated with each one of the plurality  
5     of independent ~~instruction~~multi-packet threads are unique.

1     18. (original) The apparatus according to claim 9, further comprising: a bi-directional access port  
2     operationally connected to said analysis machine; an input buffer operationally connected to said  
3     analysis machine; and an output buffer operationally connected to said analysis machine.